POWER ELECTRONIC TRANSFORMER DEVICE MODEL BASED ON DSP PROTECTION

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Abstract - Space Vector Pulse Width Modulation (SVPWM) technology has higher voltage utilization, lower instantaneous rate of change and smaller total harmonic distortion than Sinewave Pulse Width Modulation (SPWM), and is more suitable for digitization To achieve, so more and more attention. SVPWM technology can be applied to cascaded multilevel converters to achieve lower voltage fluctuation and smaller harmonic distortion. It can be seen from the simulation and experiment that SVPWM technology can be applied to cascade Multi-level converter, the output voltage fluctuation rate is small, the overall utilization rate is higher.

Keywords: Power Electronic Transformer; Bidirectional Active Full Bridge DC-DC Converter; H Bridge.

1. Introduction

With the rapid development of distributed generation micro-grid technology, high bandwidth communication technology and Internet technology, the concept of smart grid has been put forward at home and abroad. It is different from the conventional power grid in terms of generation, transmission, distribution and power consumption because the energy of the traditional power grid is transmitted to the user side in one way, while the smart grid can realize the two-way transmission of energy, services and information between the user side and the grid side. Smart grid is a new modern power supply system, which can realize the process of system monitoring, protection and information transmission [2].

AC-DC-AC topology has three different levels.

The first stage is called high voltage input stage, mainly composed of three-phase voltage source PWM converter. Its main control objective is to control the power factor on the network side and the energy can flow in two directions. Its main goal is to control the DC bus voltage on the input side of the intermediate stage.

The second stage is called medium-voltage intermediate stage. The main function of the isolated bidirectional active full-bridge DC-DC converter is to convert high-voltage direct current into high-frequency medium-voltage direct current. Because of the existence of transformer, it can realize electrical isolation, making it have the same function as traditional transformer [3].

The third stage is called low-voltage side output stage, which mainly uses three-phase voltage source PWM inverters. Low-voltage input stage has many forms, such as three-phase four-wire structure, three-phase four-leg structure, three-phase three-wire structure, and single-phase inverter structure.

Although these topological forms are different, the analysis methods are similar.

Using intelligent electronic power transformer to replace the traditional transformer in substation can reduce the use of some secondary equipment, thereby reducing the cost. It not only can realize the functions of traditional transformer, such as transformer, isolation and energy transfer, but also realize flexible power control and power quality regulation.

Therefore, studying the intelligent power electronic transformer has important research significance and research value for development of the intelligent substation [4].

2. Principle and Structure

2.1. Basic structure and working principle

Figure 1 shows the difference between smart grid and conventional grid [1]. In Figure 1, the advanced metering infrastructure (AMI) mainly corresponds to the AMR (automatic meter reading) of smart meters.

The information collected by the measurement system is transmitted to users and the power grid to achieve two-way interaction. Advanced distribution operations (ADO) corresponds to system monitoring and distribution management system, provides demand response auxiliary services, and realizes the interaction mechanism between renewable energy and dynamic energy storage system of electric

vehicles. Advanced transmission operation (ATO) corresponds to energy management system. Energy transfer of photovoltaic power station and offshore wind farm is realized through flexible high voltage direct current transmission (HVDC) converter station and other devices [2]. Power electronic transformer system has many forms, as shown in Figure 2.

It consists of three-phase bridge pulse-width modulation (PWM) rectifier circuit, single-phase power transformer, single-phase bridge PWM rectifier circuit, single-phase bridge inverter circuit, and three-phase bridge PWM inverter circuit.

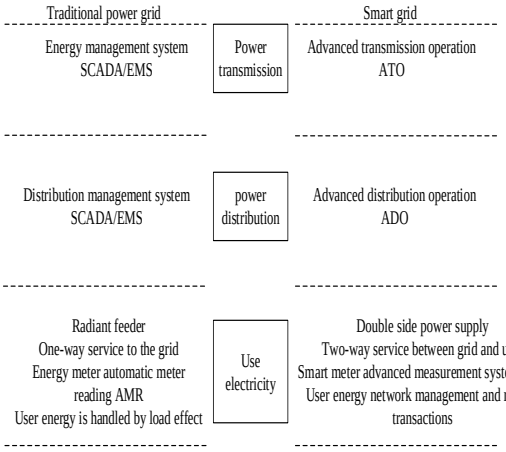


Figure 1: Contrast between traditional grid and smart grid

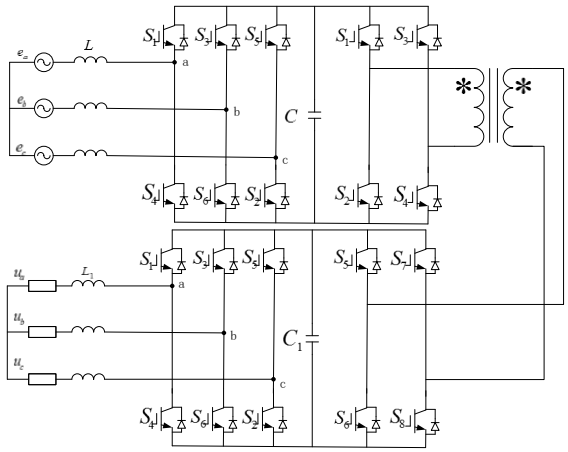


Figure 2: Topological structure of power electronic transformer

The basic working principle of power electronic transformer is shown in Figure 3.

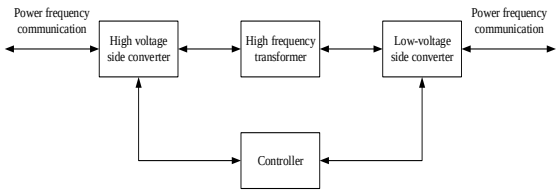


Figure 3: Basic working principle of power electronic transformer

The power frequency alternating current first passes through the high voltage side converter of power electronic transformer to the high frequency square wave signal, which is the input signal of the primary side. Then, the high-frequency transformer couples the input signal of the primary side to the secondary side, and then converts the low-voltage side converter into the customized power required by the user.

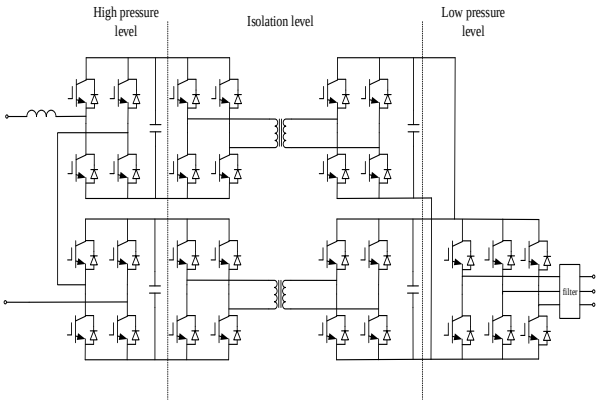


Figure 4: Structural schematic diagram of two-stage cascaded power electronic transformer

The main circuit topology of two-stage cascaded power electronic transformer is shown in Figure 4. It consists of three parts: the front stage high voltage rectifier stage, the intermediate stage high frequency isolation stage, and the post-stage low voltage inverter stage. The front stage high voltage rectifier is made up of H bridge in series, i. e. cascaded H bridge. Cascaded H bridge can get the only AC port, which is connected to the grid side [5]. The DC side of the rectifier is connected by each H-bridge rectifier of the cascaded H-bridge independently and separately with its corresponding separate isolation stage circuits.

The intermediate isolation stage consists of a front H bridge (single-phase inverting bridge), a high frequency transformer, and a rear H bridge (single-phase rectifying bridge). The intermediate isolation stage is connected one to one with cascaded H-bridge converters. The DC side of the front H bridge and the DC side of the cascaded H bridge converter of the front high voltage stage correspond to the connection circuit respectively. The primary side of the high frequency transformer is connected with the AC side of the front H bridge, and the secondary side is connected with the AC side of the rear H bridge. The DC side of the rear H bridge is connected by parallel connection of the upper and lower stages [6]. It can be seen that in the topological structure of two-stage cascaded power electronic transformer, the high voltage rectifier stage and the intermediate separation stage of the single stage have the same topological structure, which can be called sub-unit.

After parallel connection of the DC side of the post-H bridge of the intermediate isolation stage, the

DC side of the post-stage three-phase half-bridge inverters is connected to the low-voltage inverters, while the AC side of the three-phase half-bridge inverters is connected to the three-phase load.

Because the current voltage withstanding level of power electronic devices is not enough, cascade power electronic transformers are needed to improve the voltage level. In general, the cascade series of power electronic transformers is determined according to the level of the power network they are connected to.

2.2. Two-stage cascaded H-bridge PWM rectifier

In order to make the system withstand higher power and voltage, the two-stage cascaded H-bridge PWM rectifier is adopted in the high-voltage input stage, and its topology is shown in Figure 5.

Two-stage cascaded H-bridge PWM converter is connected to the power grid through filters. Its main function is to convert the AC current of the power grid into two independent and stable DC currents.

Its main control objectives are: to reduce the input current filter; the power factor of the input current is 1 or -1; the DC side voltage of the two-stage H-bridge converter remains the same, and the numerical value is equal to the set value [7].

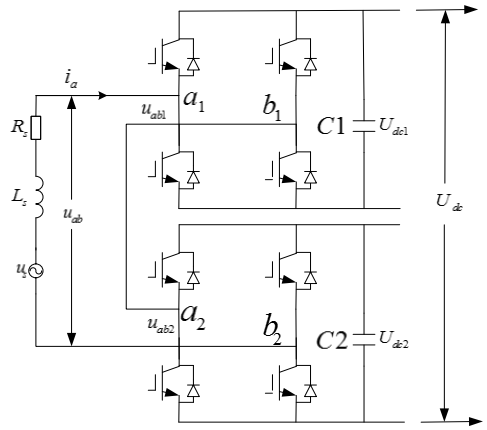


Figure 5: Structural schematic diagram of two-stage cascaded H-bridge PWM rectifier

Before analysing the two-stage cascaded H-bridge PWM rectifier, it is necessary to analyse the working principle of H-bridge converter, and its topology is shown in Figure 6.

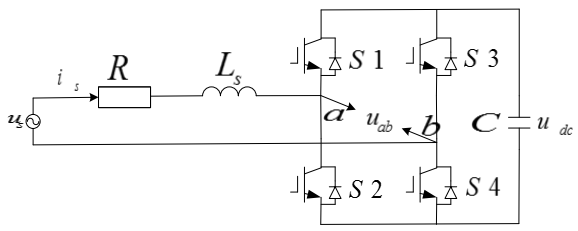


Figure 6: H-Bridge PWM converter topology

In the figure, S1~S4 represents the driving signals of four switches, L is the filter inductance, R is the equivalent resistance of the filter inductance, C is the DC side capacitor, u_{ab} is the input voltage of the inverter side, u_s is the grid voltage, i_s is the grid current, and u_c is the DC output voltage.

Assuming that the voltage source, inductance, switching device and capacitor are all ideal components, the mathematical model of single-phase PWM converter can be obtained according to Kirchhoff voltage law.

$$u_s = Ri_s + L\frac{di_s}{dt} + u_{ab} \tag{1}$$

$$u_{ab} = S_k \cdot u_{dc} \tag{2}$$

In the formulas, S_k represents the switching function.

$$S_k = \begin{cases} 1 & S_1, S_4 \text{Conduction} \\ 0 & S_1,\ S_3(S_2,\ S_4)\ \text{Conduction} \\ -1 & S_2,\ S_3 \text{Conduction} \end{cases} \tag{3}$$

The equivalent circuit of single-phase PWM converter can be obtained from Formula (2) as shown in Figure 7.

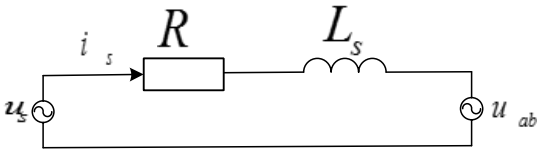


Figure 7: Equivalent circuit of H-Bridge PWM converter

Formula (1) and Figure 7 show that the size of u_c can be controlled by controlling the size of i_s; at the same time, by controlling u_{ab}, the network side current i_s and the power factor of the system can be controlled.

The topology of two-stage cascaded H-bridge PWM rectifier is shown in Figure 4, and its mathematical model can also be established.

Firstly, the following assumptions are made: switching devices are ideal devices, switching losses and switching time are neglected; network inductance and DC side capacitance are ideal components and there are no inductance saturation problems; the design parameters of upper and lower H bridge modules should be the same; network side voltage source should be ideal sinusoidal voltage source.

Among them, u_s and i_s are the voltage and current on the grid side, L_s and R_s are the inductance and line resistance on the grid side, C_1 and C_2 are the DC capacitance on the upper and

lower cascaded H-bridge, u_{ab1} and u_{ab2} are the AC voltage on the input side of the upper and lower H-bridge modules, U_{dc1} and U_{dc2} are the DC voltage on the upper and lower H-bridge modules, and u_{ab} and U_{dc} are the total AC voltage at the input side and the total DC voltage at the DC side of the two-stage cascaded H-bridge, respectively.

The switching functions of the upper and lower H-bridge modules are represented by S_{1k} (k = 1, 2, 3, 4) and S_{2k} (k = 1, 2, 3, 4), and there is:

$$S_1 = \begin{cases} 1 & S_{11}, S_{14}\text{Conduction} \\ 0\, S_{11},\ S_{13}(S_{12},\ S_{14})\ \text{Conduction} \\ -1 & S_{12},\ S_{13}\text{Conduction} \end{cases} \quad (4)$$

$$S_2 = \begin{cases} 1 & S_{21}, S_{24}\text{Conduction} \\ 0\, S_{21},\ S_{23}(S_{22},\ S_{24})\ \text{Conduction} \\ -1 & S_{22},\ S_{23}\text{Conduction} \end{cases} \quad (5)$$

The voltage equation of the circuit obtained from KCL and KVL is as follows:

$$\begin{cases} u_{ab1} = S_1 \cdot u_{dc1} \\ u_{ab2} = S_2 \cdot u_{dc2} \end{cases} \quad (6)$$

$$u_{ab} = u_{ab1} + u_{ab2} \quad (7)$$

$$u_s = Ri_s + L\frac{di_s}{dt} + u_{ab} \quad (8)$$

From Formula (8), it can be found that the equivalent circuit of H-bridge two-stage cascaded PWM converter and H-bridge PWM converter are basically the same, as shown in Figure 7.

Similarly, as shown in Figure 7 and Formula (8), the DC side voltage can be controlled by controlling the magnitude i_s of the voltage; at the same time, the network side current i_s and the power factor of the system can be controlled by controlling u_{ab}.

2.3. Structure and principle of DAB converter

The intermediate isolation stage consists of a front H bridge (single-phase inverting bridge), a high frequency transformer, and a rear H bridge (single-phase rectifying bridge), and its topological structure is shown in Figure 8.

High frequency transformer plays an important role in energy transmission, voltage change, and electrical isolation.

Meanwhile, it determines the size of the power electronic transformer.

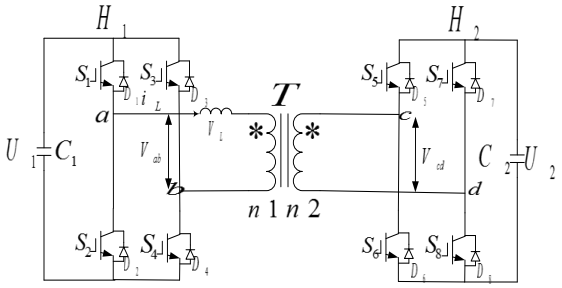


Figure 8: Topology of bidirectional active bridge DC-DC converter

The following expressions for transformers are given in the literature:

$$A_e \bullet A_c \propto \frac{VA}{B_m \bullet f \bullet J} \quad (9)$$

Among them, VA is transformer capacity, unit: VA; Ae is winding effective area, unit: m^2; Ac is core area, unit: m^2; B_m is the maximum flux density, unit: T; f is excitation frequency, unit: Hz; J is conductor current density, unit: A/ m^2.

In the engineering design of transformer, the variation range of maximum flux density and excitation frequency is very small, so the change of both can be ignored. Therefore, from Formula (9), it can be considered that the product of winding coil area Ae and core area Ae is inversely proportional to frequency.

Therefore, in the design of transformer, the frequency of transformer can be reasonably increased to reduce the volume and weight of transformer.

3. Logic and Algorithm of Electronic Power Transformer Protection System

3.1 Protection logic and algorithm

For protection system, the main function of logic and software system is to monitor system parameters, and identify and classify different faults. When the fault occurs, different measures should be taken for different faults and different severity, such as maintaining normal operation, fault alarm or fault shutdown.

Due to the use of a large number of power electronic components and power electronic conversion technology, the protection software needs to analyse and convert the input and output of the switch and the sampling signal of the device.

Because of the complexity of hardware configuration in the protection system of electronic power transformer, it is impossible to quickly and accurately analyse data and distinguish and locate faults if the software system cannot cooperate well.

If so, not only the research and development and production cost of the protection system is high, but also some faults may be omitted and neglected, resulting in the incomplete protection system and affecting the overall performance of the protection system, thus affecting the normal operation of the entire electronic power transformer system.

Therefore, according to the characteristics of the hardware protection device of the electronic power transformer in distribution network, it is of great significance to develop the transformer protection software which can be applied to reduce the maintenance cost and the reliability of the protection system. Based on the hardware protection system of 10kV/400V0.5MVA distribution network electronic power transformer, the software system scheme suitable for it is studied. The new protection technology scheme for electronic power transformer is fully considered, including the design of monitoring software, the protection scheme for different operation states, the protection logic design, and the design of monitoring system and the upper computer. The protection software based on this scheme has been debugged and applied to the electronic power transformer of 10kV/400V 0.5MVA distribution network.

The protection program can perform two kinds of actions according to the magnitude of the operation condition exceeding the rated value, namely, fault alarm and fault shutdown. When the monitoring and protection system detects that the protected object has reached the fault alarm value in a control cycle, it will enter the fault alarm. The specific processing method is to display the alarm information continuously on the host computer screen and the screen of the monitoring and protection chassis [8].

When the value of the protected object returns to normal in the next cycle, the display of the alarm information will be cancelled, but the fault alarm record of the host computer still exists. In order to reduce the impact of interference on the monitoring and protection system and avoid false alarm and malfunction, when the monitoring and protection system detects that the protected object has reached or exceeded the upper limit (or lower limit) of the malfunction downtime value in a sampling period, it will not immediately execute the malfunction downtime procedure, but start counting through the counter. When the count is three times, it will be confirmed that the fault is not interference to the transformer or AD port, and then the fault shutdown program will be executed. If the monitoring and protection system detects that the protected object has returned to the normal range before the counter has been counted three times, the counter will be reduced by 1. In this way, the burr detected by AD digital and analog chip in the sampling process can be eliminated as far as possible, and the influence of actual value or other interference on the monitoring and protection system can be mistaken.

After the control system of the electronic power transformer is powered on, the monitoring and protection system checks the control system and the main circuit of the electronic power transformer.

The self-checking of the control system is mainly aimed at the DSP, and the checking mode and process of each DSP board are exactly the same, while the checking of the main circuit state is different because different DSPs correspond to different parts of the main circuit. The self-checking program of the control system mainly checks the external function modules of the DSP board. Only when these modules can work properly can the follow-up program run [9]. If an exception is detected, the fault is returned and displayed on the chassis screen and the host computer. The self-checking results show that all the extended function modules on the DSP board can work normally before they can enter the next step of the main circuit self-checking. The state checking program of the main circuit is slightly different for each DSP. The monitoring and protection DSP in the monitoring and protection chassis and the DSP in the controlled auxiliary chassis need protection checking, while the input-level control DSP board and the output-level control DSP board in the monitoring and protection chassis do not need the main circuit checking.

After self-checking of control system and main circuit, the system will enter standby state. At this time, the system allows the electronic power transformer to accept the start-up instructions.

At this time, various control and protection parameters of the system can be modified in the host computer, that is, the parameter management function mentioned above. It should be pointed out that if the system fails to self-check through the main circuit before, it will enter the fault state. If it does not do any troubleshooting, it can still enter the standby state by issuing the reset command directly (press the reset button on the cabinet door). However, because the fault still exists, it will still be checked out in the subsequent self-check-start and cannot start. Therefore, this design will not avoid the protection system starting with fault due to mis-operation, thus bringing hidden dangers to the system. At the same time, the protection system has certain flexibility by pressing the reset button to enter the standby mode. If the input voltage is under-voltage due to other subjective reasons (e.g. the system needs to operate in low voltage environment, so the input voltage cannot be self-checked through the main circuit), then the reset key can be pressed to the standby state in the fault state, and then the protection parameters can be modified, such as reducing the rated value of the input voltage

in the input voltage protection to the input voltage currently provided, or modifying the upper or lower stopping limits of the protected object.

Because many parameters of the system are unstable during soft start-up, it is not suitable for normal operation protection. For example, when the input current is soft start, the DC bus capacitor is charged, so it may exceed the upper limit of over current protection. The output AC voltage may be lower than the lower limit of the output voltage under-voltage protection because the DC bus voltage is not charged to the rated voltage. At this time, the abnormal output current and voltage waveform may affect the sampling of the frequency and phase of the output voltage, making the frequency and phase protection action. At the same time, in the soft start process, charging current or DC bus voltage may oscillate repeatedly due to various reasons, which eventually leads to the soft start process timeout and other issues. At this time, it is necessary to protect the system to suspend the soft start-up process, trip and shut down. After eliminating the problem, it restarts [10]. In summary, due to the uncertainty of system parameters during soft start-up, it is necessary to design a protection program for soft start-up process separately. After pressing the start-up button on the cabinet door panel, the electronic power transformer changes from standby state to start-up state. In the start-up state, start-up protection should be carried out first, mainly for checking and judging the start-up conditions, so as to avoid the system starting under abnormal conditions. The start-up condition is satisfied, that is, the start-up program can be started only after the protection is started. Start-up conditions to be met include input voltage to meet the requirements, input voltage frequency to meet the requirements, output voltage and current to zero, all circuit breakers are in the open state, without any failure signs that have not been cleared, etc. [11].

When the electronic power transformer is in operation, the system will execute the shutdown logic if the shutdown button on the cabinet door panel or the monitoring and protection program is pressed to detect serious faults and request the shutdown. The shutdown logic first stops sending trigger pulses of input stage rectifier to make the input stage rectifier work in the state of uncontrolled diode rectification, and at the same time causes the voltage of DC bus to drop. Then, it stops sending trigger pulses of output stage inverters to prevent the power flow in the main circuit of electronic power transformer and avoid the fault expansion. After that, the output circuit breaker, input circuit breaker, and charging resistance circuit breaker are disconnected. When the monitoring protection board confirms that the three circuit breakers are in the open state, the output stage inverter drive pulse is reproduced, and the DC capacitor is discharged by the fan hanging on the output stage.

When the DC bus voltage of output stage is reduced to a set value, the driver pulse of output stage inverter and the isolation stage chopper pulse are stopped, and the shutdown procedure is terminated. Because this process involves the synchronization and communication of 9 DSPs in 4 control chassis, it is complicated and complex to implement. It is necessary to confirm whether the lock pulse or open pulse signal has been received between the monitoring protection board and the auxiliary chassis control board repeatedly.

When the shutdown button is pressed on the cabinet door, the system will enter the standby state after the shutdown, waiting to modify the system parameters or restart. The system will refuse to accept any modification parameters and start-up commands, and the system must be reset after troubleshooting before it can enter standby state.

In the case of failure, the failure indicator of the cabinet door will always be on, and the display screen of the monitoring and protection cabinet and the upper computer will show that the system is in a failure state. When the reset button on the cabinet door is pressed after troubleshooting, the system will clear the registers such as the current fault marker, soft start marker, soft start delay counter, button marker and various fault counters and enter the standby state, waiting for the soft start command or parameter modification command [12].

If failures cannot be eliminated in the state of failure, the reset key can still be pressed to reset the system, but after soft start by pressing the start key, the start-up protection will be checked. If the start-up is successful, the normal operation protection will also be carried out after that, and the system may fail again.

3.2 Monitoring system technical solution

The design of monitoring software includes communication function, LCD display function and keyboard function. Its design requirements are as follows: window interface and menu design and keyboard function design; communication with DSP board (CAN communication); LCD display content; fault analysis function, including fault display, fault recording, and fault analysis; parameter management.

Parameter management mainly includes parameter initialization, update, save, and consistency check. As mentioned above, system parameters should be initialized before starting self-test. System parameters are stored in two different addresses in EEPROM. When initializing parameters, the two parameters are read out and compared together. If they are not consistent, the parameters in EEPROM cannot be used by electronic power transformer, but must be initialized by default parameters.

After obtaining the system parameters, the corresponding variables of the control program and the monitoring and protection program should be assigned according to the meaning of each parameter in the system parameters, so as to realize the initialization of the system parameters.

In standby state, the host computer can update various parameters. Firstly, the host computer sends the value of the variable needed to be modified to the DSP through the CAN bus, and then the control parameters are saved in the control parameter array, and the control parameters used in the control program are updated directly.

Meanwhile, the parameters in the monitoring and protection program will be saved to the array of control parameters instead of updating directly to the application program.

Only when the DSP receives the command to complete the modification of parameters, these parameters will be updated to the monitoring and protection program.

Technically, the control parameters can be modified at anytime and anywhere, and the monitoring and protection parameters can only be modified in standby state.

The execution frequency of the parameter saving program is different from 600Hz of the main control program, which is 50Hz, that is, implements once 20ms. CAN (Controller Area Network) communication mainly uses the way of query to transmit and receive data.

The frequency of DSP receiving control parameters and commands from the host computer is 50Hz, that is, query per 20ms; while the frequency of DSP sending state variables, control parameters, event records, experimental records and accident records to the host computer is 1.67ms, that is 600Hz.

Accident record is of great significance to accident analysis, diagnosis, maintenance, and maintenance significance of control system. Its main contents are various state variables.

Accident records are usually triggered by abnormal signals in the system, such as over-voltage and over-current signals or manual triggers.

The time range of recording is generally 5-10 seconds before and after triggering time, and the time rate is 10ms to 20ms, respectively.

Since the memory of the controller generally does not have the power-off protection function, the contents of the memory will be lost after the power-off of the system, so the accident record should be read out from the host computer to the hard disk of the host computer through the serial port as soon as possible.

When the accident record is transferred to the host computer hard disk, the accident record in the controller memory should be deleted in time.

Otherwise, because the memory capacity is small, it will affect the later accident record storage.

In order to realize the function of accident recording, it is necessary to set up a cyclic change data storage pointer and point to the accident data storage area in the NVRAM extended by the special DSP board.

When the accident record program is triggered, the accident record termination pointer is calculated, the data pointer and the termination pointer are compared, and the record is kept until the two are equivalent.

That is to say, the accident record does not start after the accident occurs, but continuously records data in normal operation, and then stops after the accident occurs for 10 seconds.

The data storage period of the accident record is 10ms, and the data is stored for 12 seconds, 2 seconds before the accident, and 10 seconds after the accident. In order to record the response curve of electronic power transformer under the change of input voltage and load in field or laboratory tests, manual trigger test records are needed to debug the control of the device.

Therefore, in order to realize the function of experiment recording, it is necessary to set data storage pointer to the special SRAM storage area.

When the trigger signal of the experimental record is sent out, the data will be recorded continuously for a certain period of time.

When the data storage is completed, the trigger signal of the experimental record will be cleared.

The storage period of the data recorded in the experiment is 1.67ms, i.e. the storage frequency is 600Hz.

In addition to the accident record and experiment record, the monitoring system also designs the event record function, which mainly records the time when the operation, protection, alarm and other states occur or terminate, such as switch displacement and status mark displacement, so as to facilitate the analysis of the system operation status and accident causes.

The program only has two functions: clearing event record and uploading event record.

In order to fully monitor the important status flags, each of the input and output registers of the switching quantity will be monitored.

When one of them changes, it means that an event occurs.

Although the event records of input level control motherboard, output level control motherboard and monitoring protection board are different, they can be divided into three categories: command event, start event, and monitoring protection event.

Command events are generally related to the host computer, usually referring to the receipt of a command or the completion of a command; while start-up commands are related to various changes of state flag bits in the soft start process, such as DSP self-checking success flag bits, main loop self-checking flag bits and so on; monitoring and

protection events mainly refer to the detection of various state variables, such as overvoltage and over current.

4. Design of Experimental Platform for Two-Stage Cascaded Power Electronic Transformer

4.1 Hardware design of two-stage cascaded power electronic transformer experiment system

Figure 9: (1) IGBT module F4-100R12KS4

Figure 9: (2) Intelligent Power Module (IPM)PM300DVA120

As shown in Figure 9, the high-power switching devices used in the front high-voltage rectifier stage and the intermediate high-frequency isolation stage are single-phase full-bridge type and IGBT module.

The model of the TGBT is F4-100R12KS4, which is manufactured by Infineon. The inner part of the TGBT module is an H-bridge circuit connected by four IGBT switches. In addition, the voltage withstand value of the IGBT is 1200V, and the maximum current allowed to pass through is 100A.

The circuit of the laboratory can withstand the circuit of 60A at most, so the IGBT module can fully meet the requirements of the laboratory. In addition, because the module is an H bridge, it constitutes the basic module of power electronic transformer.

Three-phase PWM inverters are used in the low-voltage inverters of power electronic transformers.

The model used in the test is PM300DVA120. The module is a three-phase half-bridge inverter switching device and its manufacturer is Mitsubishi Company of Japan. The module can withstand a maximum voltage of 1200V and a maximum current of 300A. The switching frequency of IGBT switching unit in the module is up to 20kHz, and the minimum dead time is 3.5u, which can fully meet the requirements of verification experiments. Since there are two IGBT switching units in a single IPM module, three IPM modules are needed to form a low voltage inverter stage. It should be noted that an inductance-free capacitor is needed between the DC buses of each module.

The function of the inductance-free capacitor is to absorb the switching-off surge voltage and recover the surge voltage by the continuous-current diode.
In addition, the parameters of LC filter circuit are three inductors, $L_a = 1219\ \mu H$, $L_b = 1210\ \mu H$, $L_c = 1255\ \mu H$ and capacitance parameter $C = 47 \mu F$. Each DC side of the system needs to be connected with a DC capacitor. The function of the capacitor is to stabilize the voltage and the size of the DC capacitor is 450V/100000 μF.

H-bridge is the main power module of the two-stage cascaded power electronic transformer's front-stage high voltage rectifier stage and intermediate separation stage. Therefore, the development of H-bridge driving circuit board has become the most important thing. The IGBT module used in the development of H-bridge driving circuit board is F4-100R12KS4 of Infineon Company of Germany. The rated voltage of the power module is 1200V and the rated current is 100A. For the driver chip of power module, the chip of type 2ED020112_FI is chosen here.

The internal structure of 2ED020112_FI chip mainly includes level conversion element, logic input element, coreless transformer, under-voltage protection element, a general comparator, and a general operational amplifier.

The 2ED020112_FI chip is a gate driver for high voltage and high speed voltage power switching devices. It has two interlocking outputs, which are independent, so one chip can drive two switches. When the voltage between VSH and VSL is between 13V and 18V, the driver chip runs normally.

If the voltage is too low, the under-voltage protection unit inside the chip starts to work, and the driver chip does not work at this time.

The drive capability of the suspended high voltage side is achieved by guiding the diode and capacitor. In addition to each driving logic input element, the logic input element uses Schmidt trigger circuit, which has good anti-interference ability.

The 2ED020112_FI chip is also equipped with a special shutdown input.

All logic inputs are compatible with 3.3V and 5VTTL levels.

When the level of the/SD port is low, it will send a signal. InH and InL ports no longer accept the pulse type, so the circuit forms self-locking protection.

In addition, when the level of the/SD port is high, if the InH is high and the lnL is low, then the OutH can work normally. Conversely, if InH is low and InL is high, OutH can still work normally. If both InH and InL ports are high-level, the chip will not work inside until one of the two ports becomes low-level.

The output drive characteristic of the chip in the high pulse current buffer stage is designed for the lowest drive on.

This universal operational amplifier can be used to detect IGBT in the lower arm of H bridge. It is specially designed for fast detection, and the reaction time is greatly reduced. The input of the amplifier can detect the voltage between - 0.1V and 2V, and the output stage is ±5mA. The general comparator can be used for current detection with IGBT. Considering the internal security of the chip, a pull-up resistor and a pull-down resistor are introduced at the input ends of the universal comparator.

In order to form an isolation barrier between the lower driver and the upper driver in the transmission process and to avoid the mutual interference of signals, CLT (Computer Language Translation Program) coreless transformer is adopted here. Coreless transformers send signals from coded transmitters after special coding to the corresponding receiver at the other end. In this way, electromagnetic interference due to changes in GNDH (dVGNDH/dt) or flux density (dH/dt) will be suppressed. It should be noted here that in the process of signal transmission, signal receivers, coreless transformers and compensating transmitters have delays. Due to compensating transmitters, receivers and coreless transformers will have delays in the process of signal transmission. In order to solve this problem, a professional propagation delay is introduced into the lower arm.

The main function of the control signal driving circuit is to transmit the PWM pulse signal from DSP to the IGBT module. Since the maximum voltage of the used DSP 2812 is 3.3V, the photo-coupler isolation between the DSP and IGBT should be added. The photo-coupler TLP250 is a totem pole output, so there is no need for up-resistance at Vcc and Vo terminals, so it is more convenient to use. The driving circuit of PWM pulse signal from DSP2812 to TGBT passes through two-stage inverter 4049 and two-stage photo-coupler TLP250. In the process of using photo-coupler TLP559, pull-up resistance is needed, and the resistance value of this pull-up resistance should be as small as possible.

But if the pull-up resistance is too small, it will lead to excessive current, which will affect the service life of components.

At the same time, the rise and fall time of TLP250 is much smaller than that of TLP559. Considering comprehensively the function of level conversion and isolation, TLP250 is chosen here.

The experimental platform built is a two-stage cascaded power electronic transformer, in which the IGBT module F4-100R12KS4 of Infineon is used for both the front and intermediate separation stages. The driver chip used is 2ED020112-F1 produced by Infineon, so the control signal needs to be sent to the input of the driver chip.

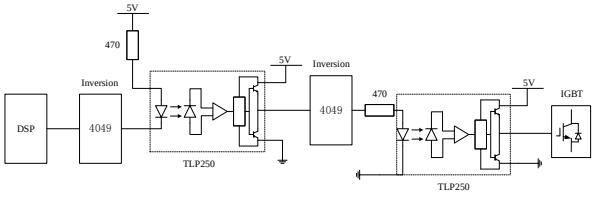


Figure 10: Control signal driving circuit

In the experiment, the voltage and current signals of the system need to be collected in real time to control the system well. Therefore, the design of sampling circuit should take into account the practical application, should have the ability to operate under various conditions, and be easy to use. The electrical signals that the sampling circuit needs to collect are voltage and current, so voltage and current sensors are needed.

If the maximum measured current is positioned at 100A, the current sensor type chosen is LA100-P.

The rated current of the primary side is 100A and the rated current of the secondary side is 50mA, and the ratio is 2000:1, so there are:

$$\frac{I_{IN}}{I_{OUT}} = \frac{I_{IN}}{U_{OUT} \cdot R_M} = 2000 \tag{10}$$

The conversion coefficient is obtained as follows:

$$K_A = \frac{I_{IN}}{U_{OUT}} = \frac{2000}{R_M} \tag{11}$$

If the measuring resistance is 100Ω, it can be obtained:

$$K_A = \frac{2000}{R_M} = \frac{2000}{100} = 20 \tag{12}$$

Select the type of voltage sensor LV25-P.

The rated currents of the primary and secondary sides are 10mA and 25mA, respectively, and the ratio is 1:2.5. There are:

$$\frac{I_{IN}}{U_{OUT}} = \frac{R \cdot I_{IN}}{R_M \cdot I_{OUT}}, \frac{I_{IN}}{U_{OUT}} = \frac{1}{2.5} \tag{13}$$

R_M is measuring resistance and R is current limiting resistance. The conversion coefficient may be as follows:

$$K_V = \frac{I_{IN}}{U_{OUT}} = \frac{R}{2.5 \cdot R_M} \tag{14}$$

When R =100kΩ, R_M is 200Ω, then the following formula can be obtained:

$$K_V = \frac{R}{2.5 \cdot R_M} = \frac{100000}{2.5 \cdot 200} = 200 \tag{15}$$

The BNC terminal used in this experiment platform is used as the data transmission tool from sampling circuit to DSP controller. Compared with BNC with 50Ω, this model has strong current absorption and anti-interference ability.

4.2 DSP software design

TI company's main product, TMS320F2812 DSP, is used as the main control chip. It is 32-bit fixed-point DSP chip.

The main frequency of CPU is 150MHZ. Table 1 is its detailed parameters.

Table 1. DSP2812 parameters

Name	Parameter	Name	Parameter
Instruction cycle	6.67ns	A/D conversion unit	380V/50Hz
Interrupt level	3-level	Watchdog Timer	1
Input/output voltage	3.3V	In-chip RAM	18K*16 bits
Maximum AD sampling frequency	12.5MSPS	CPU timer	3
In-chip Flash	128K*16 bits	External interrupt	3
I/O	56	Serial communication interface	2
Time manager	2	Analog/digital channel	16

In power electronic transformer, the operation control of the whole system is based on DSP, which is the center of the whole system. The block diagram of the control circuit is shown in Figure 11.

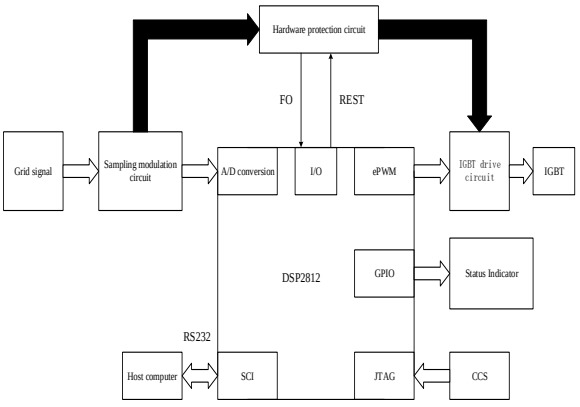


Figure 11: Block diagram of control circuit

Its main functions are: real-time acquisition of voltage and current signals in the system to achieve A/D conversion of electrical signals; communication with the host computer through SCI serial port; fault protection such as over-current and over-voltage; generation of PWM wave signals, and control of IGBT after IGBT driving circuit.

The main function hierarchy of the DSP program is shown in Figure 12. Figure 12(a) shows that the main program enables enabling global interruption enter the main loop after system initialization, PE control register, interrupt vector table initialization, EV event manager initialization and GPIO port setting.

As can be seen from Figure 12(b), the main cycle program mainly consists of several parts: real-time acquisition of voltage and current signals in the system to achieve A/D conversion of electrical signals, calculation of actual electrical signals, determination and protection of circuit over-current and over-voltage faults, control strategy algorithm, generation and update of PWM wave signals and interruption parts.

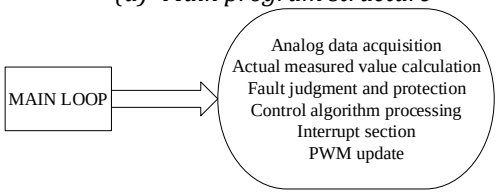
From Figure 12(c), it can be seen that the control strategy algorithm is mainly composed of four parts: normalization processing, calculation of directional triangular function, PI controller, and coordinate transformation.

Figure 12(d) shows that interruption mainly includes TINTO, T1PINT, XINT1, McBSP interruption, PWM interruption and SCI communication interruption.

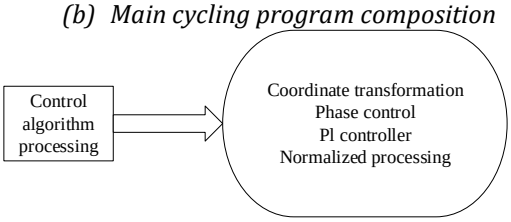
The main program flow chart is shown in Figure 13.

```
main()
{
InitsysCtrl();          //Initialize system DINT;
1nitPieCtrl();          //Initialize the PIE Control Register
InitPieVectTable();     //Initialize the PIE interrupt vector table
InitGpio();             //Set up GPIO
InitEV();               //Initialize the event manager
EINT;                   //Enable global interrupt
for (;;)                //Main loop
{
MAIN LOOP
}
}
```

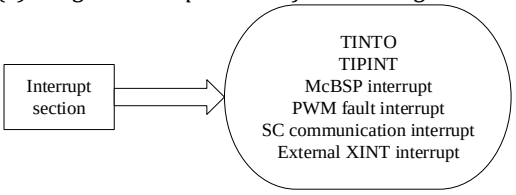
(a) Main program structure



(b) Main cycling program composition



(c) Program composition of control algorithms



(d) Interruption composition

Figure 12: Hierarchical structure diagram of principal function

When the EV event manager is initialized, the value of TMODE is defined as 1, so that the counting mode of universal timer T1 becomes continuous increment/subtraction counting mode. AD sampling is realized by AD7656 chip on the development board of DSP. The chip is a 16-bit successive approximation ADC chip, which has six channels.

The chip has a resolution of 0.305mV. If the conversion efficiency is considered to be u, the actual input analog voltage is u * 0.305mV. The frequency of power grid is 50Hz. It can be known from the H-bridge control strategy that the coordinate of single-phase system cannot be changed due to the lack of a degree of freedom. The usual method is to simulate an orthogonal quantity with 90 degrees of phase difference. In the DSP program, the amount of fictitious voltage is achieved by the number of historical data searched by array. In order to reduce the number of error sampling points, the amount of fictitious voltage should try to be an integer. Taking the aβ detection method as an example, the sampling frequency of 9kHz is adopted, so that the sampling points corresponding to the phase difference of 90 degrees are 45 integers. If the sampling frequency of 10kHz is selected, the phase difference between the two adjacent sampling points is 1.8 degrees, so the corresponding sampling points are decimal, which will cause larger errors.

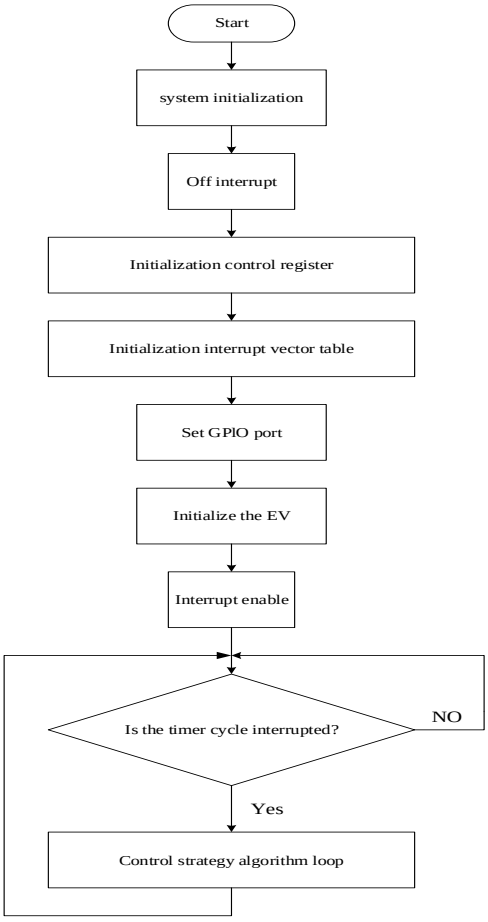


Figure 13: Main program flow chart

It can be seen from the above that DS program mainly includes: electrical signal acquisition program and control strategy algorithm program, interruption subroutine and communication interface program, determination and protection program that detects the actual electrical signal value calculation program and circuit over-current and over-voltage fault. Among them, determination and protection program that detects the actual electrical signal value calculation program and circuit over-current is available after the sampling circuit collects the information of the electrical signal.

5. Conclusion

Power electronic transformer has the advantages of interconnection, high degree of control freedom, high frequency electrical isolation, and adjustable power factor. Therefore, the research on power electronic transformer is of great significance for the development of smart grid. The main points are as follows: For H bridge grid connection, a new grid connection method is proposed. Compared with the traditional dq decomposition method and aβ detection method in MATLAB/Simulink simulation, the results show that the proposed method has shorter delay time. The control strategies of two-stage cascaded power electronic transformer are analysed, and the model is built on MATLAB/Simulink and simulated.

The simulation results show the effectiveness of the proposed control strategy. The experimental platform of power electronic transformer is developed, mainly its hardware circuit, such as H bridge driving circuit board and auxiliary circuit, and the software part of the experimental platform - the software design of DSP, is analysed. The proposed control algorithm is transplanted to the DSP processor.

The experiments of H-bridge interconnection, two-stage cascade H-bridge interconnection, and DAB interconnection are carried out using the hardware platform. The voltage single-loop control experiment of three-phase half-bridge inverter is also carried out. The experimental results verify the effectiveness of the proposed control method.

A two-stage cascade power electronic transformer experimental platform is built, which has some shortcomings in withstanding voltage and withstanding power. The further improvement of this paper includes: the experiment is carried out under low voltage environment, and the voltage level can be improved in the future; the two-stage cascade power electronic transformer experimental platform is built, and its high voltage DC side has only two H bridges for cascade. If there are more H-bridge cascades, the DSP cannot control them.

The cooperation of FPGA and DSP can be used to realize the control of multi-level cascaded H-bridge.

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