KEY TECHNOLOGY DESIGN OF VIRTUAL INSTRUMENT FOR FAULT DETECTION ON ANALOGUE INTEGRATED OPERATION-AMPLIFIER BASED ON FPGA AND DSP

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Abstract: Based on FPGA and DSP chips, the detection circuit, which has four key technical indexes of analogue integrated operational amplifier, is designed. According to the fault dictionary method, the fault cause and fault position of the integrated operational amplifier can be judged, which proposes a new method for analogue circuit fault diagnosis. A design scheme of several key parts is given. They respectively are the design of the Excitation source circuit module, the design of the information acquisition and transmission module of FPGA, the circuit design of the key parameter test module, and the design of the DSP chip and the PC machine module. Through the overall system circuit test, it has achieved a good test result, and it has solved the problem of analogue integrated operational amplifier fault diagnosis, and also provides some technical support for analogue PCB board fault diagnosis.

Keywords: Fault Diagnosis; FPGA; Fault Dictionary Method; Integrated Operational Amplifier

1. Introduction

Since twentieth century, with the rapid development of electronic technology, EDA technology continues to develop and update under the promotion of the new technology. In 1990s, the standardization of hardware description language has been further established, while computer aided engineering, aided analysis and aided design have been widely used in the field of electronic technology. With the continuous improvement of FPGA processing speed, at the same time, it has been widely used in communication, computer and intelligent detection, signal processing and household appliances [1].

The development of integrated circuit design and manufacturing technology has brought great challenges to the integrated circuit fault diagnosis. At present, the development of analogue integrated circuit fault diagnosis technology is very slow, especially for the soft fault diagnosis of analogue element parameter deviation, there is no unified practical method [2, 3]. Most of the existing analogue circuit fault diagnosis research is aimed at two terminal components such as resistors and capacitors, but it is difficult to diagnose the faults of integrated operational amplifiers in the circuit. In view of this problem, we use FPGA and DSP chip as the core to design each function module, and realize the fault detection of the integrated operation-amplifier through the common function of each function module [4,5]. The related information of the chip is sent to the DSP chip through the PC, and then sent to the integrated operation- amplifier test module after DSP processing. The test module stores the control code and the test code, and the test code is sent to the test chip to produce the corresponding response. The test module collects the response and sends it back to DSP. After processing by DSP, the corresponding information is sent back to the PC computer and compared with the information of the chip in the database. If the two are the same, the chip is normal. If it is different, the chip is damaged. With the rapid development of FPGA/CPLD device, it is widely used in data acquisition, data processing and other fields due to its fast running speed and high reliability. A test system of analogue integrated chip based on FPGA (Altra FLEX10K) is introduced.

2. System Overall Design

According to the requirements of analogue integrated operation-amplifier fault detection, the test system consists of five basic modules: The PC upper computer module is responsible for the establishment of fault dictionary data and the judgment of faults. DSP module is responsible for the collection of test chip data. FPGA module is

responsible for the processing and transmission of DSP data acquisition. The test module is responsible for testing and collecting the key parameters of the analogue integrated operational amplifier.
The excitation source module is responsible for providing the excitation signals needed to test each module. The specific block diagram is shown in figure 1.

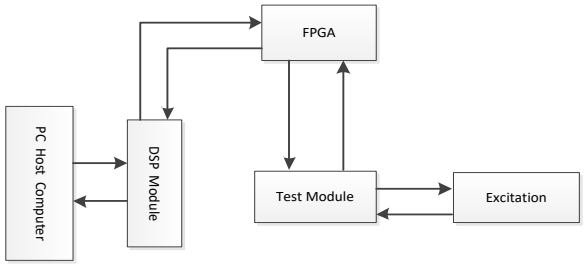

Figure 1: Hardware structure of the tester

According to figure 1, an example is proposed to better illustrate the work flow of the tester. If we want to test the B494 chip, PC first sends B494 to DSP for processing, and then sends the control signal to FPGA decoding after processing. On the one hand, the FPGA generates the enable signal of the driver chip B494, and sends a determined test code (B494 excitation) with Vcc=15V and Io=1mA (pin 7) to the test board of integrated operation-amplifier for storage.

On the other hand, the control signal produced by FPGA writes the excitation signal to the integrated operation-amplifier test board. According to the control signal control, the pin 12 of the B494 is Vcc=15V, and the input current is controlled Io=1mA with pin 7 grounded power supply. At the same time, the control panel collects the response of the pin 14 (Vref) and sends the response back to the DSP.

Finally, the response is returned to the PC. It is compared with the information of the chip in the database (data in the database is 4.91V to 5.91V).
If the former is in the range of the latter, the voltage of the chip B494 is normal.

3. Information acquisition based on FPGA and design of transmission module

According to the overall requirements of the tester, a function module based on FPGA is designed, which can process, collect and transmit data according to the information sent by DSP [6].

In order to meet the information requirements sent by DSP, the integrated operation-amplifier test board based on FPGA can be divided into three modules: ①decoding module; ②data acquisition and processing module; ③data transmission module.

The decoding module mainly realizes the decoding of the signal generated by DSP, and generates a series of control signals to control the relevant modules in the test board. The data acquisition module is mainly used to read and write the signals sent by DSP, while it also reads and writes the output data of the measured core.

The data transmission module mainly realizes the data transmission between DSP and data acquisition, and it sends some data information to the DSP through the PC host computer. After the signal is processed by the DSP, the signal is sent to the FPGA through the address. The decoding module of FPGA decodes the signal and generates a series of control signals. At the same time, according to the requirements of DSP, the work of data transmission module and data acquisition module work is controlled for the data transmission and acquisition. The hardware design is shown in figure 2:

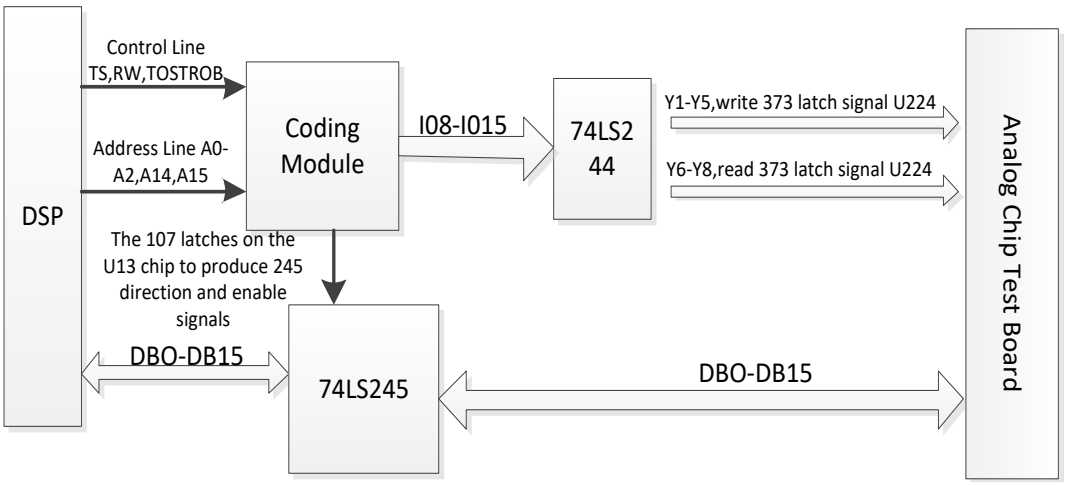

Figure 2: FPGA signal acquisition and transmission module diagram

4. Module design of test circuit

The test circuit module mainly realizes the automatic measurement function for several key parameters of analogue integrated operational amplifier.
Two groups of relays are used to control the circuit state and realize the automatic measurement of the parameters. The first group is the main measuring circuit part. As shown in figure 3, since the measurement of BWG and TR requires the different circuits, we add two relays to facilitate switching between the two circuits.

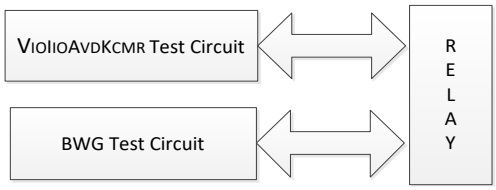

Figure 3: Principle diagram of automatic measurement

$$V_{o1} = -\frac{R6}{R7} * V_S = -V_S = A_V * V_{i1} (V_{o1} = V_{o2}) \quad (1)$$

4.1 Measurement of open loop amplification

As shown in figure 4, the whole circuit constitutes a large loop negative feedback. The signal is input according to "virtual short" and "virtual-off" feature. Because the upper end of the R7 is connected to the noninverting end of the amplifier and it is the ground potential, the electric potential of the node OUT1 is:

$$V_{i1} = V_{o2} * \frac{R1}{R1 + R2} \quad (2)$$

(V_{o2} is the output voltage of the amplifier U2)
Obtain:

$$V_{o1} = A_V * V_{o2} * \frac{R1}{R1 + R2} \quad (3)$$

$$A_V = \frac{V_{o1}}{V_{o2}} * \frac{R1 + R2}{R1} = -\frac{V_S}{V_{o2}} * \frac{R1 + R2}{R1} \quad (4)$$

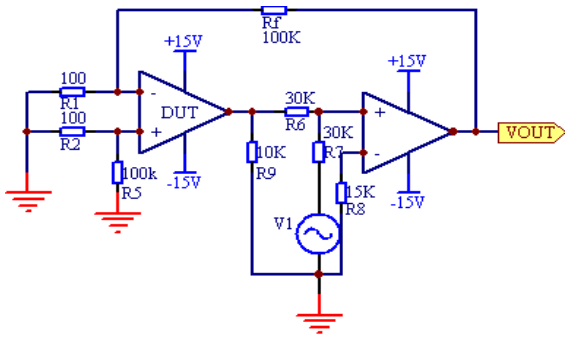

Figure 4: Measuring principle diagram of open loop amplification

4.2 Measurement of input offset voltage

As shown in figure 5, the output of the amplifier U1 is connected to the noninverting end of the amplifier U2 through a resistor divider network, while the inverting terminal of the amplifier U2 is grounded.

Therefore:

$$V_{o1} = 0 + 0 * \frac{R6}{R7} = 0 \quad (5)$$

According to the definition of input offset voltage, the following formula is obtained:

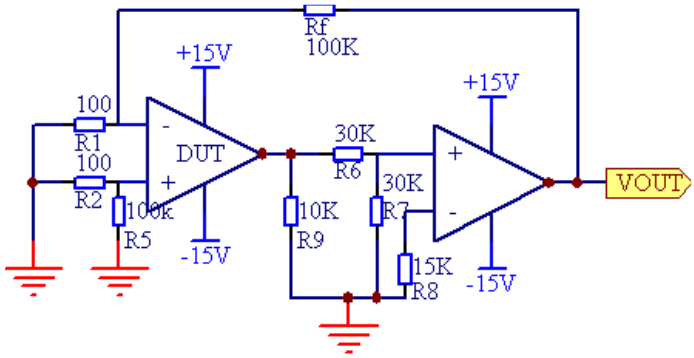

Figure 5 Test schematic diagram of input offset voltage

$$V_{OS} = V_I = V_{o2} * \frac{R1}{R1+R2}(V_{o1} = 0) \quad (6)$$

$$I_{OS} = \left(V_L * \frac{R1+R2}{R1} - V_{IO}\right) = (V_{L2} - V_{L1}) * \frac{R1}{R1+R2} \quad (7)$$

4.3 Measurement of input offset current

As shown in figure 6, the formula is:

same as the expression mentioned above, that is $V_{01}=0$ therefore,

$$V_{IO} + I_{OS} * R + V_L * \frac{R1}{R1+R2} = 0 \quad (8)$$

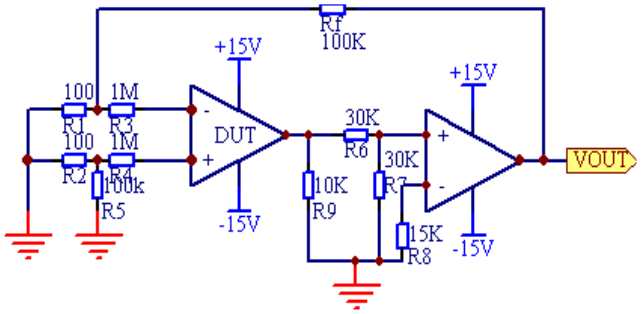

Figure 6: Schematic diagram of input offset current test

4.4 Measurement of common mode rejection ratio

The op amp should have a strong ability to suppress common mode signals. The parameter that characterizes this capability is called the common mode rejection ratio, expressed in KCMR.

It is defined as the ratio of the differential mode voltage gain AVD to the common mode voltage gain AVC, that is KCMR=|AVD/AVC|. The test principle is shown in figure 7. Because of RF>>RI, the gain of the closed-loop circuit to the differential mode signal is AVD= RF/RI, and the gain of the common mode signal is AVC=(VO/VS). Therefore, the common mode rejection ratio can be obtained only when the VO and VS are measured from the circuit. The size of KCMR=|AVD/AVC|= （RF/RI）*（VS/VO）KCMR is often related to frequency, but also related to the size and waveform of input signal. The frequency of measurement should not be too high, and the signal should not be too large [7].

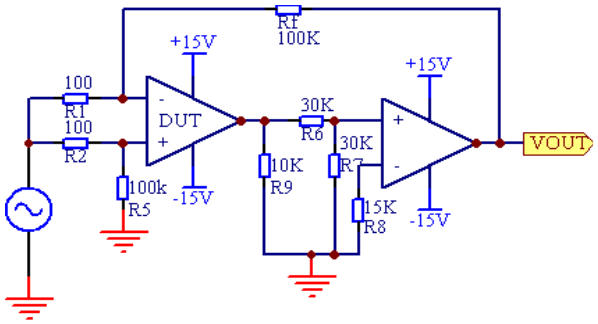

Figure 7: Measurement schematic diagram of common mode rejection ratio

5. Design of DSP chip and PC module

In the virtual instrument for fault detection on analogue integrated operation-amplifier, the system hardware is divided into PC host and executive circuit board. The PC host is the main control, and the execution circuit board takes DSP as the core to form the executive circuit. DSP is mainly responsible for data transfer of PC host computer in the integrated operation- amplifier test board.

The workflow is summarized as follows: The PC sends the test command, and the DSP chip is responsible for receiving the test command. DSP sends some of the information to the field programmable gate array (FPGA) through the address line and generates control signals for the integrated operation- amplifier test board [8]. At the same time, when FPGA produced "read" signal is received, The DSP chip transmits the excitation required by the integrated operation- amplifier from the data transfer bus to the test board of amplifier through the device 74LS245, and the information will be buffered. When the excitation is sent to the chip to be tested, the chip generates corresponding response, and the corresponding test data also exists in the test board of the integrated operational amplifier.

When the "write" signal from FPGA is received, the collected data is sent back to the DSP chip through the bidirectional transceiver 74LS245. The DSP chip deals with the signal and transforms it into an identifiable signal for the PC, and sends it back to the PC host computer. The main control PC carries on the analysis and judgment to the data transmitted by DSP and the database, and draws the conclusion to achieve the purpose of fault detection [9].

5.1 Design of communication protocol between PC host computer and DSP chip

Whether it is PC or DSP, if user wants to transmit data to each other, they must first send a request signal (one byte: 0x99), and receive the reply signal (one byte: 0x88) before they can start the transmission.

5.1.1 Transmission of test command of operation- amplifier (PC—>DSP)

Frame header＋identification code + control signal mode ＋check code + end of frame

1Byte	1Byte	Byte	1Byte	1 Byte
0xa5	0xa2	DB31~DB0		0x5a

Taking uA741 as an example (sending data from DB31 to DB0), DB31~DB0=000D123E is obtained according to the operational test coding method of the document (revised version V2.0). Check code: the number of bytes that are different from or after the byte of the identifier and the control signal pattern is used as the check code. That is, check code =0x83, so a frame of data is: A5A2000D123E83 5A.

5.1.2 Transmission of test command of operational amplifier（PC<—DSP）

Frame header＋identification code + output value of measured operational amplifier＋check code + end of frame

1Byte	1Byte	2Byte *	1Byte	1Byte
0xa5	0xa2			0x5a

*Note: After setting the decimal point, there are 4 significant digits, for example, the voltage value is 4.5268V, then the number is multiplied by 10000 before the transmission (eliminating the decimal point), which is 45268. 0xB0D4 is represented in sixteen-hexadecimal, and this is the final transmission data. PC receives this frame value and compares it with the maximum value stored in the database. If the value is less than the maximum value, it is correct, otherwise there is a fault.

5.2 Implementation of serial communication between DSP chip and PC

Considering the convenience of hardware connection and software programming, the MAX3111 serial asynchronous transceiver is directly connected with the MCBSP of DSP in the virtual instrument of integrated operation-amplifier fault detection.

The hardware does not require any other peripheral devices. Because the sending and receiving of asynchronous data is realized by MAX3111 in hardware way, the synchronous data communication between DSP and MAX3111 is considered in software programming.

In this way, the synchronous and asynchronous serial data format conversion can be realized by the simplest hardware connection and software programming. The hardware connection is shown in figure 8, and the flow chart of the software programming is shown in figure 9 [10].

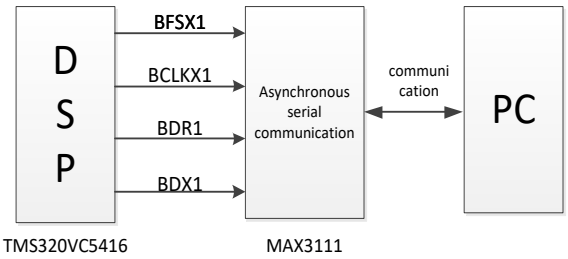

Figure 8: Hardware schematic diagram of serial communication

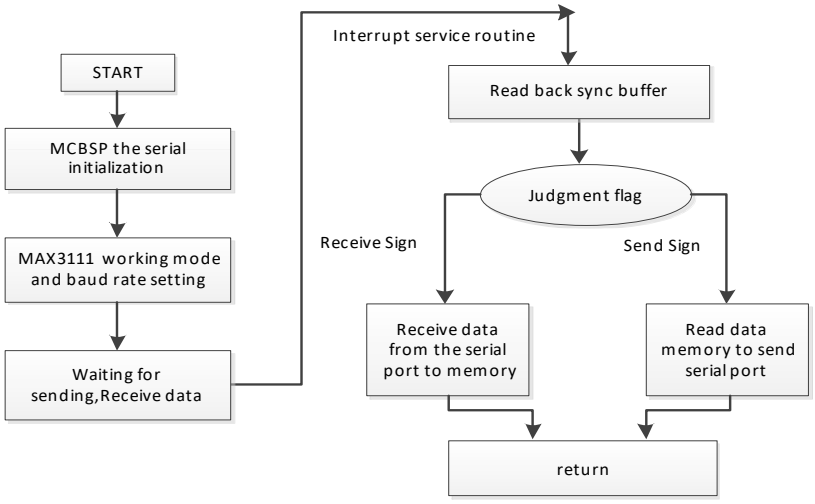

Figure 9: The simplest flow chart of serial communication

6 Conclusion

In this paper, an analogue integrated operation-amplifier fault detector based on FPGA and DSP is designed, and the performance test for the analogue test parameters of the integrated operation-amplifier is realized. Meanwhile, through the FPGA data transmission and acquisition, as well as the DSP chip, the control function of PC host computer to the test board of integrated operation-amplifier is realized. In addition, the test information transfer and sampling data acquisition and judgment are completed. Several important modules in the integrated operation- amplifier fault detector are designed in this system, and good results are obtained after unified debugging.

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