MODELLING THE INTERWOVEN PARALLEL TESTING PROCESS IN THE AUTOMOTIVE INDUSTRY

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Abstract – *This paper presents an original contribution regarding the improvement of the automatic EOL (End of Line) parallel testing process of electronic control units (ECU) in the automotive industry, by implementing an interwoven parallel testing algorithm to increase the testing quality. The new interwoven parallel test algorithm groups the tests into parallel test groups through which the defect of the pins in the connector is detected and at the same time allows the tests to be performed through the parallel test algorithm of all inputs and outputs. It combines the advantages of reduced test time with the detection of defects on the pins. The last part of the paper highlights the results obtained through the modeling of the interwoven testing algorithm and presents our conclusions that emerge from this case study.*

Keywords: End of Line, Device Under Test, Parallel Group Test, Interwoven test groups, Input, Output, Algorithm, Production, CAN.

1. Introduction

It is known that the testing time of electronic control units (ECU) at the EOL (End of Line) test station is optimized by the parallel typing algorithm compared to traditional testing.

The authors, in the paper "Modelling of the automatic testing process of electronic control units in the automotive industry", describe in detail the optimized test algorithm, where all inputs and outputs are grouped together and tested in parallel [1]. This algorithm comes to support the paper "Contributions to the modeling of manufacturing processes for the implementation of the Kanban methodology in the automotive industry" in which the authors present a modeling of the manufacturing processes for the implementation of the Kanban methodology by optimizing the processing time at the EOL test station [2].

Although parallel testing presents a series of advantages through the drastic decrease in testing time resulting from the grouping of inputs and outputs, it has the major disadvantage that it can very easily mask pin defects.

If a pin is bent for various reasons, it may touch one of the adjacent pins in the connector and will cause a short circuit between it and its neighbor.

A first conclusion consists in the fact that the parallel test algorithm cannot determine the adjacent inputs from the same connector if they are short-circuited. Figure 1 shows an example of a DUT (Device Under Test) together with its connectors.

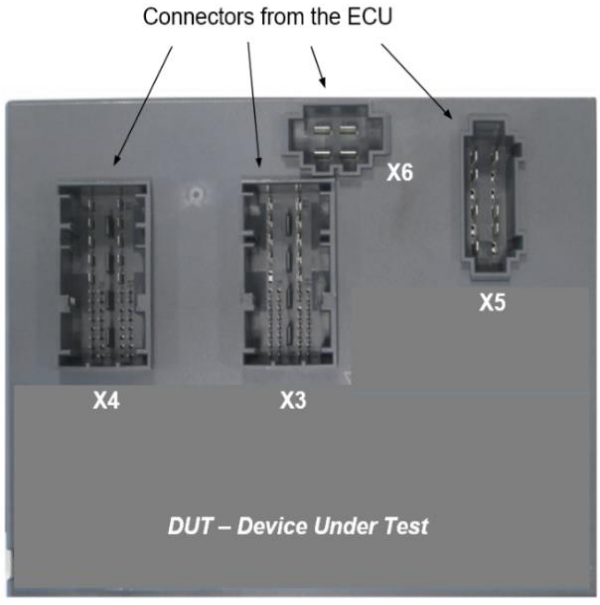


Figure 1: The connectors from the DUT

The connector marked X5 supplies the ground terminals (KL31) from the car chassis which is connected to the negative terminal of the car's 12V battery.

The X6 connector supplies the 12V (KL30) supply lines from the car's battery. Together, the X5 and X6

connectors provide the ECU with electrical power for the proper operation of the electronic component.

The X3 connector makes the connection and is responsible for the input of the electrical signals from the sensors, and on the X4 connector the electrical output signals from the ECU are mapped to the electrical actuation elements of the actuators.

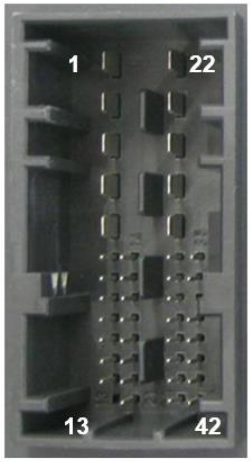
Even if the suppliers of Tier-1 electronic equipment perform rigorous electronic tests at the functional test station, some defects can sneak up to the end customer. That is why it is necessary that the study and implementation of the test steps be handled with responsibility to avoid the additional costs associated with defective units returned from the customer [3].

In order to ensure the necessary time to launch on the market, solid requirements are needed for comprehensive and additional checks to ensure the quality of the products [4].

The pressure in the business in the automotive industry comes primarily from the competition of project managers and test engineers who must ensure the good quality of the finished products. Because some of the ECUs are critical for the proper functioning of the car, thorough testing should not be discounted, despite the higher costs to ensure the desired quality in order not to endanger the lives of the traffic participants [5].

2. Case Study

The electronic tests that are carried out at the EOL (End of Line) test station for validating the quality of the electronic product are strictly carried out on the DUT connectors from figure 1. For a better representation of a connector, it is presented in figure 2 a) and b) an example of modeling for it.



1		22	
2		23	
3		24	
4		25	
5		26	
6	14	27	35
7	15	28	36
8	16	29	37
9	17	30	38
10	18	31	39
11	19	32	40
12	20	33	41
13	21	34	42

a) Picture connector b) Connector modeling

Figure 2: The connectors from the DUT

To be able to refer more easily to the position of the pins, each pin in the connector in figure 2 a) corresponds to a cell in the table shown in figure 2 b).

The parallel testing algorithm of all inputs specifies that they are stimulated in the OFF state, that is, they are disconnected from the stimuli. Then the DUT is interrogated on the communication channel how it "feels" the inputs and its response is compared with the values specified by the test requirements. If the answer is valid, then it continues with the stimulation of the inputs in the ON state. The response from the DUT is also read through the communication channel and compared with the response expected by the test specifications.

This algorithm of parallel testing of all inputs has only one weakness. If a pin is bent, it may touch its neighbor, causing a short circuit.

Taking for example pin X3-11, pin 11 in the X3 connector, in figure 3, was bent for various reasons.

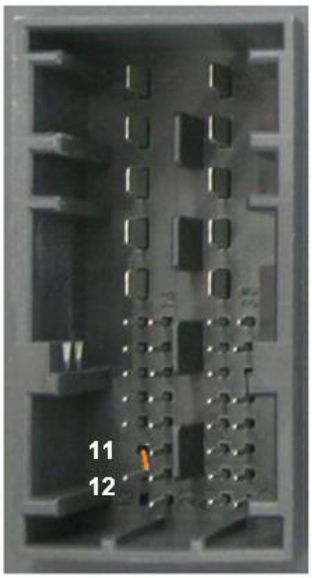


Figure 3: Pin X3-11 bent from the X3 Connector

It is most likely that during the previous operation, at the assembly process station of PCB A (Printed Circuit Board Assembled) with the case, a problem occurred, and pin X3-11 was bent.

The functionality of the connector is simple. It must make electrical contact between the ECU pins to which it belongs, and the surrounding world. If this minimum requirement cannot be met, then the system no longer works, potentially having disastrous consequences [6].

From figure 4, it can be seen that the pin X3-11 is disconnected from the stimulus of the test system (ESZ Switch 4) due to the bend and is connected in parallel with X3-12 due to the short circuit caused by the bent pin X3-11. After stimulation in the OFF state of all inputs in parallel, they will be disconnected, even the X3-11 input is disconnected from the stimulus because it is also in parallel with the X3-12 input.

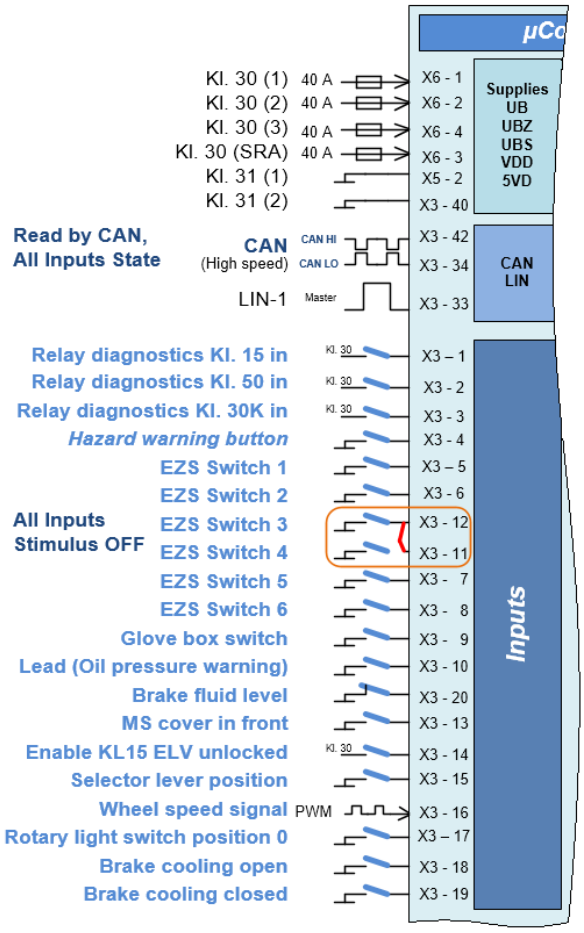


Figure 4: Stimulation of all the inputs in the OFF state [1], X3-11 bent to X3-12

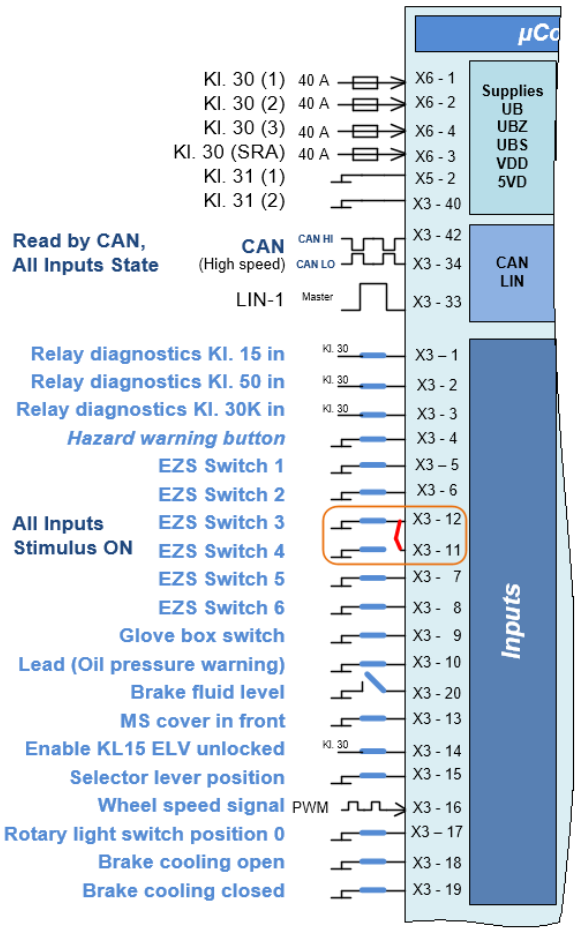


Figure 5: Stimulation of all the inputs in the ON state [1], X3-11 bent to X3-12

Following the DUT's query on the communication bus, it is found that all the inputs are detected as being in the OFF state, which results in a valid test with the test requirements, even in the case of the X3-11 input which is "stimulated" being in in parallel with X3-12. The test result of input X3-11 is wrongly marked as PASS.

Figure 5 shows the parallel testing of all inputs in the ON state. All the inputs are stimulated in the ON state, but due to the interruption of the path from the switch "ESZ Switch 4" to the X3-11 input, the stimulus no longer reaches this input. However, due to the short circuit between X3-11 and X3-12, the X3-11 input will be stimulated by the "ESZ Switch 3" stimulus applied to the X3-12 input.

This fact constitutes a false stimulus for X3-11 which goes against the principles of testing. The response of the DUT for input X3-11 stimulated in the ON state, will be valid, even if X3-11 is disconnected from the stimulus.

Following the analysis of the parallel testing algorithm of all inputs, it turns out that short-circuit defects of the inputs can be easily masked, and the biggest problem can occur when an ECU with at least one input interrupted and short-circuited with another, reach the end customer.

There are situations in which there is a defect in connector X4 in figure 6, at the bent pin X4-39.

Figure 6: Pin X4-39 bent from the X4 Connector

In this case, the output pins must also be analyzed from the point of view of short circuit faults. As in the parallel test algorithm described in [1], all the electrical loads are connected on the output lines of the DUT and then by the CAN (Controller Area

Network) command, all the outputs are deactivated at once. Then, on each individual output, the voltage at its terminals is measured and compared with the requirements of the test specifications. If the voltages on each input are close to the minimum potential, then everything is fine.

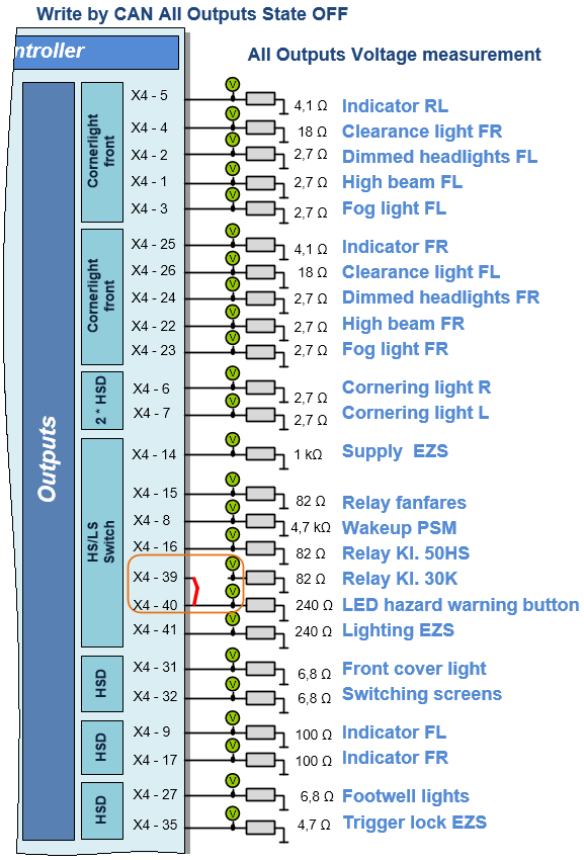


Figure 7: Stimulation of all the output in the OFF state [1], X4-39 bent to X4-40

If one of the output pins is bent, it will no longer make electrical contact with the load "connected" to its terminals.

If the output pin on a connector is bent and short-circuited with another output, for example X4-39 with X4-40, as in figure 7, the electrical voltage measured at the load terminals of 82 Ohms corresponding to pin X4-39, in this case it is 0 Volts. Same value as test specifications. For the moment, the defect is masked.

When all the outputs are tested in parallel in the ON state, stimulated on the CAN communication interface, they will be activated and therefore, their terminals must have maximum voltages.

Figure 8 shows the DUT with all active outputs in the ON state.

It can be observed that the X4-39 output, being with the bent pin, no longer makes contact with its 82 Ohm load resistance. Even if the output is active, at its related load terminals, there is no longer electrical voltage due to the lack of electrical contact. As a result, an electrical voltage will not be measured at the load terminals. This has the effect of invalidating the test for output X4-39.

It follows from here that the test step that validates the voltage measured in the ON state for the X4-39 output is FAIL. As a consequence, the defect is detected on time, without the ECU reaching the final customer.

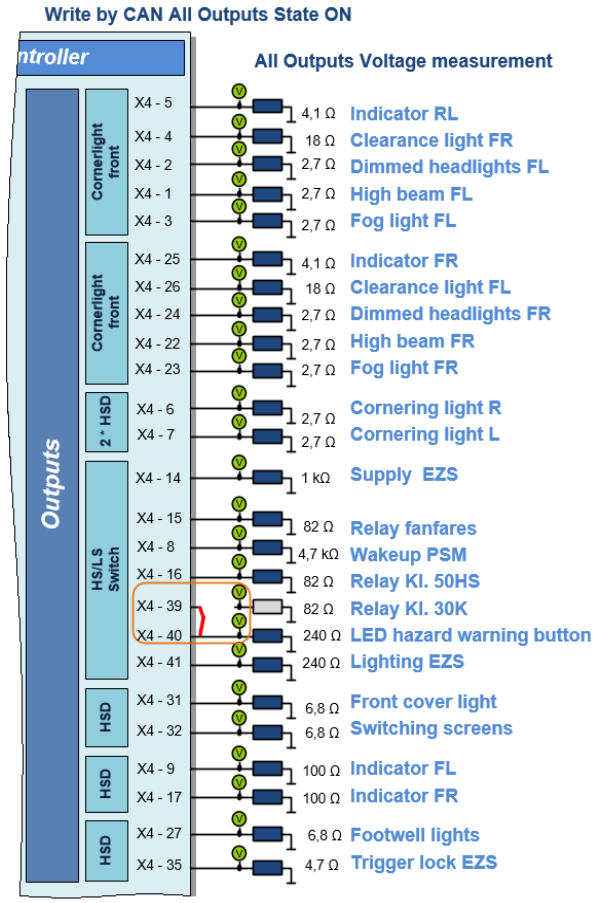


Figure 8: Stimulation of all the output in the ON state [1], X4-39 bent to X4-40

From the analysis of the 2 test scenarios of inputs and outputs, it appears that the algorithm for testing parallel inputs is not efficient from the point of view of test quality, it is only efficient from the point of view of processing speed. On the other hand, when testing the outputs in parallel, the test algorithm is efficient from a qualitative point of view and the speed of performing the tests. The advantage of the parallel testing algorithm of the inputs and the outputs was demonstrated in [1].

However, to make the parallel input testing algorithm more efficient, a new interwoven input testing algorithm is proposed.

The reconfiguration of test sequences must be done considering the configuration of the pins in the connector on which the test stimuli are applied by the test engineers [7].

3. Parallel Testing Cross Woven Algorithm

This test algorithm combines some of the advantages of the parallel input test algorithm with the order of testing the pins on each connector of the DUT.

The main idea in the new test algorithm is that the adjacent pins in the connector should not be tested in parallel at the same time. They have to be part of different groups.

Referring to image 2 (b) where the connector is modeled, by applying the new interwoven test algorithm, image 2 (b) becomes figure 9 where the pin mapping is presented on the new interwoven parallel test algorithm.

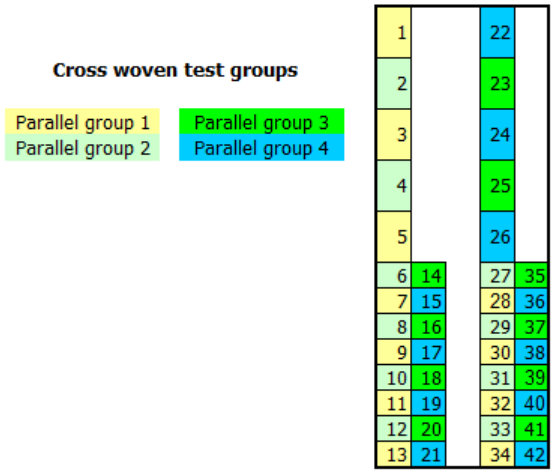


Figure 9: Mapping of cross woven tests on the connector pins

The interwoven parallel testing algorithm is divided into several distinct parallel groups and each group is tested individually with the same parallel testing algorithm.

The choice of the number of parallel groups is made taking into account the positioning of the pins in the connector.

The idea is that the adjacent pins are not included in the same test group. For this, the pins in the connector are grouped into several groups depending on the number of adjacent rows in which the pins are positioned. For example, in figure 8, there are a maximum of 2 rows of adjacent pins. Row 1 is made up of pins 6, 7, 8, 9 10, 11, 12 and 13, and row 2 is made up of pins 14, 15, 16, 17, 18, 19, 20 and 21. Taking for example pins 6, 7, 14 and 15, they cannot be present in the same parallel testing group, but must be included in 4 separate testing groups.

The maximum number of parallel groups of pins is given by the (1):

$$G = R^2 \quad (1)$$

where:

- G - the total number of parallel test groups;
- R – number of pin rows in the connector

In this case, by applying (1), the total number of testing groups becomes 4.

In figure 9, the grouping was modeled in different colors according to the position of the pins in the DUT connector.

The order of execution of the tests on the connector pins is described in detail in table 1.

Table 1. mapping pins to parallel groups

Parallel groups test	X3 connector pins
Parallel group 1	1, 3, 5, 7, 9, 11, 13, 28, 30, 32, 34
Parallel group 2	2, 4, 6, 8, 10, 12, 27, 29, 31, 33
Parallel group 3	14, 16, 18, 20, 23, 25, 35, 37, 39, 41
Parallel group 4	15, 17, 19, 21, 22, 24, 26, 36, 38, 40, 42

In the following, the 4 inter-woven parallel test groups are described.

3.1. Parallel Group 1

Testing the interwoven parallel group 1 is similar to the parallel testing of the inputs in [1]. In the first phase, the stimuli on inputs X3-1, X3-3, X3-5, X3-7, X3-9, X3-11, X3-13, X3-28, X3-30, X3-32 and X3-34 are disabled, in other words, they are set to the OFF state, as in figure 10.

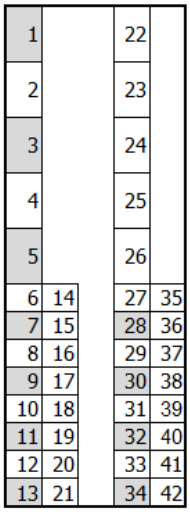


Figure 10: Parallel group 1 – State OFF

The status of the inputs mentioned above is queried on the communication bus and then the answer is compared with the template specified by the test requirements. If it corresponds, then the interwoven parallel testing algorithm continues.

Next, the inputs are stimulated in the ON state, i.e. the sensors are connected to the inputs X3-1, X3-3, X3-5, X3-7, X3-9, X3-11, X3-13, X3-28, X3-30, X3-32 and X3-34 as shown in figure 11.

On the CAN communication bus, the status of the inputs mentioned above is interrogated and the response returned on their CAN is compared with the template specified by the test requirements. In this case, the X3-11 pin is disconnected from the stimulus. At the same time, it is in a short circuit with the X3-12 pin, which is also disconnected from the stimulus because it is not tested in this group. The response returned on the CAN communication bus will be different to the expected template. In this way, the non-conformity of the X3-11 pin is detected even if it is short-circuited with the X3-12 pin. In this case, the test station detects this test step as FAIL and stops the DUT verification procedure rejecting it from the production flow.

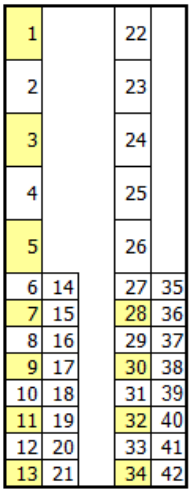


Figure 11: Parallel group 1 – State ON

Finally, the inputs are deactivated from the ON state, to the OFF state of parallel group 1 without interrogating their status on the CAN.

3.2. Parallel Group 2

Parallel group 2 repeats the actions presented in the previous sub-chapter, but for the input pins that are included in this group.

The inputs that are part of parallel group 2 are deactivated in the OFF state.

For optimization purpose, the previous operation of deactivating parallel group 1 can be executed at the same time (in parallel) with parallel group 2 as in figure 12.

Thus, the sensors from both groups 1 and 2 are deactivated and then only the parallel group formed by inputs X3-2, X3-4, X3-6, X3-8, X3-10, X3-12, X3-27, X3-29, X3-31 and X3-33 is interrogated on CAN. The response is then compared to the template specified by the test requirements.

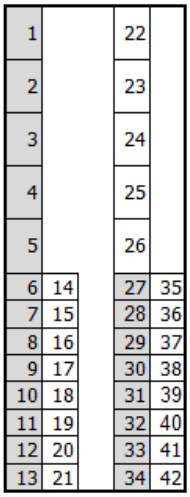


Figure 12: Parallel group 1 and 2 – State OFF

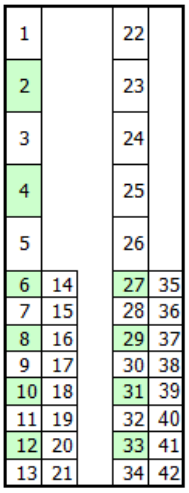


Figure 13: Parallel group 2 – State ON

The next test step is to activate the sensors on the inputs that belong to parallel group 2 as shown in figure 13.

The answer from the DUT on the CAN is compared with the pattern from the EOL test system, and if it corresponds to the expectations, then the tests are executed further.

In order to optimize the interwoven parallel test process, the deactivation of the outputs is performed in the next parallel test group.

3.3. Parallel Group 3

The parallel test group starts with the deactivation of the stimuli on the inputs of the parallel group 2 consisting of the inputs X3-2, X3-4, X3-6, X3-8, X3-10, X3-12, X3-27, X3-29, X3 -31 and X3-33.

At the same time, the inputs that belong to parallel group 3, X3-14, X3-16, X3-18, X3-20, X3-23, X3-25, X3-35, X3-37 and X3-41 are disabled as shown in figure 14.

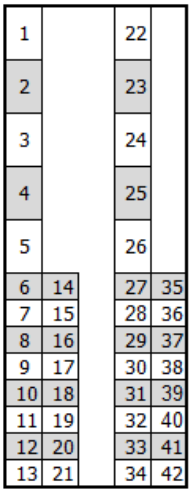


Figure 14: Parallel group 3 – State OFF

Then follows the inquiry on the CAN communication bus, the state of the inputs from this parallel group that are mentioned above. If the answer matches the expected one, then the test sequence continues.

The inputs of parallel group 3 are activated in the ON state as in figure 15.

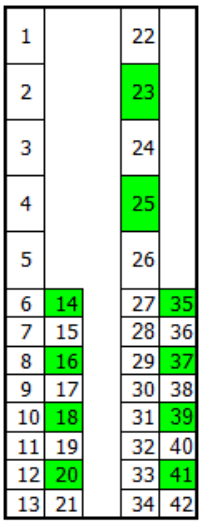


Figure 15: Parallel group 3 – State ON

On the CAN communication bus, through diagnostic messages, the response of the DUT to the stimulation of the inputs in the ON state is read, after which it is compared with the template expected by the EOL process station. If it corresponds, then the process of testing the inputs with parallel group 4 is continued.

3.4. Parallel Group 4

To test parallel group 4, it starts by deactivating the inputs of parallel group 3 consisting of pins X3-14, X3-16, X3-18, X3-20, X3-23, X3-25, X3-35, X3-37 and X3-41.

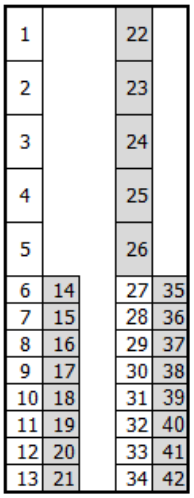


Figure 16: Parallel group 4 – State OFF 1

Then the pins belonging to parallel group 4, X3-15, X3-17, X3-19, X3-22, X3-24, X3-26, X3-36, X3-38, X3-40, and X3-42 are deactivated as shown in figure 16.

The response of the DUT to the stimulus in the OFF state of the inputs is interrogated on the CAN and compared with the response expected by the EOL test station. If everything is OK, then continue with the testing process.

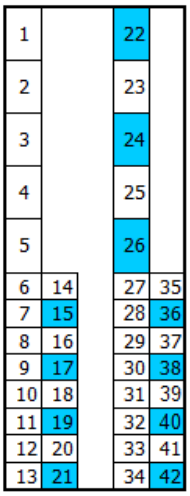


Figure 17: Parallel group 4 – State ON

The last phase of activating the inputs in the ON state is performed at parallel group 4 for testing inputs X3-15, X3-17, X3-19, X3-22, X3-24, X3-26, X3-36, X3-38, X3-40 and X3-42 as presented in figure 17.

The response of the DUT is read on the CAN communication bus and then compared if it corresponds to the requirements of the test specification.

Deactivation of the inputs from the parallel test group 4 that are already active from the previous step is deactivated in figure 18. This is the last test step where the inputs are manipulated.

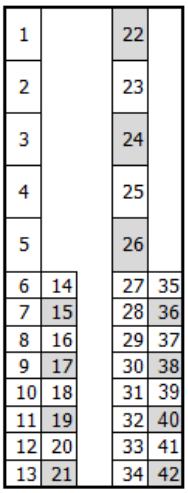


Figure 18: Parallel group 4 – State OFF 2

The inputs from this last test group 4 are deactivated in order not to introduce additional behavior of the DUT into the test process.

As a rule, after testing the functional blocks of the DUT, they are deactivated.

4. Conclusions

All DUT connectors can be tested with the same interwoven parallel test algorithm, but only after a preliminary analysis to establish the necessary parallel test groups. If the X3 and X4 connectors are similar, i.e. they have the same number of rows, then the 4 parallel test groups remain the same for the X4 connector as well.

It should be noted that the parallel group 1 in the X3 connector can be tested together (in parallel) with any of the groups that are part of other connectors. In this way, parallel testing can be performed together with other connectors.

The new proposed test algorithm brings additional cycle time for interwoven parallel testing because several groups of parallel tests must be executed. From [1] it follows that in parallel testing, where all inputs are tested in parallel, the test lasts 1.1 seconds.

If it is related to the same total number of inputs, then, with the new interwoven parallel testing algorithm, on 4 parallel test groups, the total additional testing time is described in (2):

$$(1.1\ seconds\ x\ 4) - 1.1\ seconds = 3.3\ seconds \quad (2)$$

From here it follows that the new algorithm does not negatively influence the total test time too much. Even if the processing time at the EOL station for testing the inputs and outputs increases a little, the quality of the EOL process must be in the first place. It is mandatory that the quality improvement is more important than the processing time at EOL.

It is preferable for the testing process to take a little longer than for defective electronic components to arrive at the customer, in the presented case with bent pins, in short circuit with other pins in the connector.

It also results from this that the new interwoven test algorithm has the effect of an electronic PIN Check at the EOL station.

Of course, on the production line there are process stations where the orthogonality of the pins in the connector is checked (PIN check process station), downstream from the assembly station, where the ECU case is assembled, and defects may appear.

Thanks to the interwoven parallel test algorithm, which also plays the role of electronic PIN check, important cost savings are made, because dedicated process stations for PIN check can be dispensed with.

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